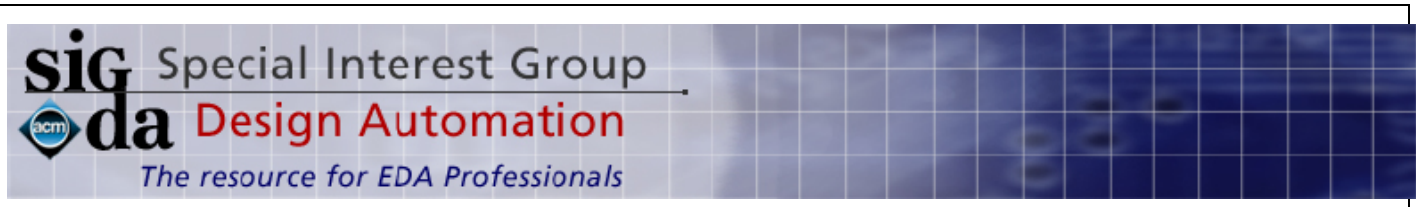
Subject: 1 February 2013 ACM/SIGDA E-NEWSLETTER Vol. 43 no. 2
From: Sudeep Pasricha <sudeep@COLOSTATE.EDU>
Date: 2/2/2013 1:42 PM
To: SIGDA-announce@ACM.ORG



1 February 2013, Vol. 43, No. 2
Online archive: http://www.sigda.org/newsletter

Comments from the Editors

Dear ACM/SIGDA members,

We are looking for new Associate Editors for SIGDA E-news. If you are interested, in the position and/or have questions about the same, please email

Sudeep Pasricha <sudeep@colostate.edu>.

In this issue, we have a very interesting article on Memristive Computing. If you are interested in contributing to this column in the future, contact Srinivas Katkoori <Sudeep Pasricha katkoori@cse.usf.edu> or Sudeep Pasricha >. An article only needs to be about 1 page long with several references. All articles are included in the ACM digital library and there is no restriction for the reproduction of the article for printed publication later.

Sudeep Pasricha, E-Newsletter Editor;
Debjit Sinha, E-Newsletter Associate Editor;
Lin Yuan, E-Newsletter Associate Editor;
Prabhat Mishra, E-Newsletter Associate Editor
Srinivas Katkoori, E-Newsletter Associate Editor

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SIGDA News

"Top 10 disruptive startup tech plays"
http://www.eetimes.com/electronics-news/4405514/Top-10-startup-articles-of-2012
If past is prologue, then a look at the disruptive technology moves of 2012 may give us some sense of what the new year will bring.

â€œStephen Hawking gets birthday gift from Intel"
http://www.eetimes.com/electronics-news/4405305/Stephen-Hawking-gets-birthday-gi...
Intel has presented Professor Stephen Hawking with a birthday gift, a 300-mm wafer with the message "Happy Birthday Stephen Hawking" inscribed hundreds of times in copper letters defined using Intel's 32-nm manufacturing procress.

"Xilinx Zynq-7000 All Programmable SoC wins Microprocessor Report Analyst Choice Award"
http://www.eetimes.com/electronics-news/4405332/Xilinx-Zynq-7000-All-Programmabl...
The folks at Xilinx are all jolly happy at the moment because their Zynq-7000 All Programmable SoC has just won the Microprocessor Report Analyst Choice Award for 2012.

"Wolfe's Den: Intel Mauls Malware with Hardware Security"
http://www.eetimes.com/electronics-news/4405171/Intel-Mauls-Malware-with-Hardwar...
In our gut, we all get that hardware-based security should outstrip the traditional, software-centric approach to antivirus protection. But does that feeling stand up to a back-of-the-napkin analysis? Well, yes.

"Facebook covets core-heavy ARM SoCs"
http://www.eetimes.com/electronics-news/4405195/ARM-SoCs--flash-don-t-match-Face...
At the same event where Facebook managers opened the door for ARM server SoCs in the data center, they also made it clear that todayâ€™s chips fall short of what they seek, In addition, NAND flash vendors need to refocus their plans to fill exploding storage needs in the data center, they said.

"Memristors mimic human brain"
http://www.eetimes.com/electronics-news/4405034/Memristors-mimic-human-brain
Memristors were conceived by electrical engineer Leon Chua in his seminal 1971 paper "Memristor--the Missing Circuit Element" (IEEE Transactions on Circuit Theory). His peer-reviewed claim startled electrical engineers by detailing how there was a "missing link" in circuit theory.

"Google edges Apple in 2012 U.S. patent race"
http://www.eetimes.com/electronics-news/4404703/Google-edges-out-Apple-in-2012-p...
Google edged out Apple in a close race to win U.S. patents in 2012. The two mobile rivals also logged the biggest gains over 2011 of any other Top 50 U.S. patent winners.

"Intel Simmers Social's Secret Sauce"
http://www.eetimes.com/electronics-news/4404190/Intel-Simmers-Social-s-Secret-Sa...
Is social media a bunch of BS? (There's a new book which argues yes.) Even if we stipulate that it's not, there's an unspoken consensus that our online interactions with the friends we've never met isn't achieving its full potential.

"Advanced capacitors ensure long-term performance stability"
http://www.edn.com/design/components-and-packaging/4405601/Advanced-capacitors-e...
To meet the demanding performance and harsh environmental conditions of automotive applications, component manufacturers have developed professional-grade tantalum capacitors that ensure long-term electrical performance stability. The professional tantalum technology satisfies the automotive industryâ€™s need for rugged capacitors that maintain high-performance standards under electrical and mechanical stress. Technical improvements have been made that strengthen the structure of the capacitor and give it more robust performance in a variety of applications.

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What is Memristive Computing?

Sangho Shin and Sung-Mo Steve Kang
University of California Santa Cruz

Continuing demands for more complex information processing require future system integration technologies to overcome various physical limitations. Of particular importance is the leakage power that is becoming a dominant limiting factor in CMOS VLSI circuits. The imminent barrier to Mooreâ€™s Law for CMOS, so called power wall, calls for revolutionary approaches for development of new devices and systems integration. To meet the increasingly more difficult technological requirements, the emergent nanoscale memristive devices have received much attention, since they provide â€˜resistanceâ€™ as a new physical state variable [1].

When the functionalities of nanoscale CMOS VLSI circuits can be integrated with the new emerging features of nanoelectronic devices, in particular the new

state variable of resistance, low-power high-performance computing systems and ultra-dense memory systems can be achieved [2]. Memristors and memristive devices have been uncovered as such devices since they can be configured into nonvolatile memories, logic gates, programmable interconnects with high integration density and, more importantly, with CMOS compatibility.

A myriad of computing circuits and systems that use â€˜resistanceâ€™ as one of the state variables [1, 4-6], e.g., memristors and memristors/CMOS hybrid [3], can be classified into the â€˜Memristive Computingâ€™ system. Memristive computing basically utilizes the emerging features of nonvolatile resistive memory devices, such as Resistive RAM (RRAM), Phase-Change RAM (PCRAM), and Magnetic RAM (MRAM).

By exploiting the nonlinear properties of nanoscale memristors, and replacing many CMOS transistors with memristive devices for latching or switching circuits, revolutionary analog/digital memristive computing can be realized with significantly reduced form factor, manufacturing cost, and active and leakage power consumptions. The promising applications of memristive computing are in
- reconfigurable nanoelectronic systems, e.g., threshold logic [7] and FPGA [8];
- resistive Boolean logic and signal processing, e.g., stateful logic [1, 4-6];
- nonvolatile VLSI computing [9]; and
- neuromorphic synaptic network [10].

Such memristive computing circuits will enable computing to be embedded into the storage system as well. In the data-intensive systems, the bottleneck is not in the compute cycles but rather in latency, bandwidth, and capacity of memory and storage accessible to a compute node. Low latency, high density memristive devices offer a unique opportunity to augment the compute node with power-efficient, high-storage capabilities [2], thus memristors that exhibit low latency and better wear characteristics will be ideally suited for a variety of data analytics tasks such as high performance scientific and national security applications.

The memristive computing primitives consume static power, though their magnitudes would be small, primarily due to the devicesâ€™ nature of voltage-current dynamics. On the other hand, leakage power can be negligible. In other words, memristive computing overcomes the basic limitation of CMOS computing which takes a significant amount of dynamic/leakage power. Such distinctive features of memristive computing units call for new CAD tools for future hybridization of memristive and CMOS VLSI systems. As such the low-cost, nonvolatile, solid-state circuit technology enabled by emerging nanotechnologies will significantly reduce the energy costs.

References

[1] K. Kim, et al., â€œField Programmable Stateful Logic Array,â€ IEEE Trans. Computer-Aided Design, vol. 30, no. 12, pp. 1800-1812, Dec. 2011.

[2] B.V. Essen, et al., â€œOn the role of NVRAM in data intensive HPC architectures,â€ Workshop on Emerging Supercomputing Technologies (WEST), May 2011.

[3] G. S. Snider and R. S. Williams, â€œNano/CMOS architectures using a field-programmable nanowire interconnect,â€ Nanotechnology, vol. 18, 035204, Jan. 2007.

[4] J. Borghetti, et al., â€œA hybrid nanomemristor/transistor logic circuit capable of self-programming,â€ PNAS, vol. 106, pp. 1699-1703, 2009.

[5] S. Shin, et al., â€œReconfigurable Stateful NOR Gate for Large-Scale Logic Array Integrations,â€ IEEE Trans. Circuits and Systems-II, vol. 58, no. 7, pp. 442-446, July 2011.

[6] S. Shin, et al., â€œResistive Computing: Memristors-Enabled Signal Multiplication,â€ IEEE Trans. Circuits and Systems-I, to appear.

[7] J. Rajendran, et al., â€œAn Energy-Efficient Memristive Threshold Logic Circuit,â€ IEEE Trans. Computers, vol. 61, no. 4, pp. 474-487, Apr. 2012.

[8] J. Cong, and B. Xiao, â€œmrFPGA: A novel FPGA architecture with memristor-based reconfiguration,â€ IEEE/ACM Int. Symp. On Nanoscale Architectures, pp. 1-8, 2011.

[9] W. Robinett, et al., â€œA memristor-based nonvolatile latch circuit,â€ Nanotechnology, vol. 21, 235203, June 2010.

[10] R.E. Pino, â€œComputational Intelligence and Neuromorphic Computing Architectures,â€ Book Chapter, Advances in Neuromorphic Memristor Science and Applications, Springer Series in Cognitive and Neural Systems, vol. 4, pp. 77-88, 2012.

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Paper Submission Deadlines

DACâ€™13 â€“ Design Automation Conference
Austin, TX
User track deadline: Feb 6, 2013
Jun 2-6, 2013
http://www.dac.com/

MSE'13 - Microelectronics Systems Education
Austin, TX
Deadline: Jan 15, 2013
Jun 2-3, 2013
http://www.mseconference.org

PACT'13 - Int'l Conference on Parallel Architectures and Compilation Techniques
Edinburgh, Scotland
Deadline: Mar 15, 2013 (Abstracts due: Mar 11, 2013)
Sep 7-11, 2013

http://www.pactconf.org

ASQED'13 - Asia Symposium on Quality Electronic Design
Penang, Malaysia
Deadline: Apr 23, 2013
Aug 23-28, 2013
http://www.asqed.org/

BIOCAS'13 - Biomedical Circuits and Systems Conference
Rotterdam, Netherlands
Oct 31 â€“ Nov 2, 2013
Deadline: Jun 14, 2013
http://www.biocas2013.org/

ICFPT'13 - Int'l Conference on Field-Programmable Technology
Kyoto, Japan
Deadline: Jun 1, 2013
Dec 9-11, 2013
http://www.fpt2013.org/

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Upcoming Conferences and Symposia

ISSCC'13 - Int'l Solid-State Circuits Conference
San Francisco, CA
Feb 17-21, 2012
http://isscc.org/

ISQED'13 - Int'l Symposium on Quality Electronic Design
Santa Clara, CA
Mar 11-13, 2013
http://www.isqed.org/

DATE'13 - Design Automation and Test in Europe
Grenoble, France
Mar 18-22, 2013
http://www.date-conference.com/

ISPDâ€™13 â€“ Intâ€™l Symposium on Physical Design
(co-located with TAUâ€™13)
Lake Tahoe, CA
Mar 24-27, 2013
http://www.ispd.cc

TAUâ€™13 â€“ Intâ€™l Workshop on Timing Issues in the Specification and Synthesis of Digital Systems
(co-located with ISPDâ€™13)
Stateline, NV

Mar 27-29, 2013
http://www.tauworkshop.com/

NOCS'13 â€“ Intâ€™l Symposium on Networks-on-Chip
Tempe, AZ
Apr 21-24, 2013
http://chatha.faculty.asu.edu/nocs2013/

NOCS'13 â€“ Intâ€™l Symposium on Networks-on-Chip
Tempe, AZ
Apr 21-24, 2013
http://chatha.faculty.asu.edu/nocs2013/

GLSVLSIâ€™13 â€“ Great Lakes Symposium on VLSI
Paris, France
May 2-4, 2013
http://www.glsvlsi.org

BSNâ€™13 â€“ Intâ€™l Conference on Wearable and Implantable Body Sensor Networks
Cambridge, MA
May 6-9, 2013
http://www.bsn2012.org

ASYNC'13 â€“ Intâ€™l Symposium on Asynchronous Circuits and Systems
Santa Monica, CA
May 19-22, 2013
http://asyncsymposium.org

ISCAS'13 - Int'l Symposium on Circuits and Systems
Beijing, China
May 19-23, 2013
http://iscas2013.org/

ViPES'13 - Workshop on Virtual Prototyping of Parallel and Embedded Systems
Boston, MA
May 24, 2013
http://www.vipes-workshop.org/

USAHOST'13 â€“ International Symposium on Hardware-Oriented Security and Trust
Austin, TX
June 2-3, 2013
http://www.hostsymposium.org/

ISCAâ€™13 â€“ Intâ€™l Symposium Computer Architecture
Tel-Aviv, Israel
Jun 23-27, 2013
http://isca2013.eew.technion.ac.il/

AHSâ€™13 - NASA/ESA Conference on Adaptive Hardware and Systems

Torino, Italy
Jun 24-27, 2013
http://www.see.ed.ac.uk/ahs2013/

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Upcoming Funding Opportunities

ASEE

Office of Naval Research (ONR) Sabbatical Leave Program
Deadline: Continuous
http://onr.asee.org/

Naval Research Laboratory (NRL) Postdoctoral Fellowship Program
Deadline: Continuous
http://www.asee.org/fellowships/nrl/about.cfm

DARPA

Defense Sciences Research and Technology
Deadline: February 7, 2013
https://www.fbo.gov/index?s=opportunity&mode=form&id=f2d279d3a55a3b4d30825429000...

Microsystems Technology Office-Wide Broad Agency Announcement
Deadline: September 1, 2014
http://www.grants.gov/search/search.do?oppId=197074&mode=VIEW

DOD

Research Interests of the Air Force Office of Scientific Research
Deadline: Continuous
http://www.grants.gov/search/search.do?mode=VIEW&oppId=158973

High Performance Computing on Massively Parallel Architectures (BAA 64-09-01)
Deadline: Continuous
http://heron.nrl.navy.mil/contracts/baa/index.htm

DOE

Director's Postdoctoral Fellows
Deadline: Continuous
http://www.lanl.gov/science/postdocs/appointments.shtml

Postdoctoral Appointments
Deadline: N/A

http://www.sandia.gov/careers/postdoc.html

Sabbaticals and Faculty Appointments
Deadline: continuous
http://www.nrel.gov/rpp/sabbaticals.html

McDonnell Foundation

Studying Complex Systems - 21st Century Science Collaborative Activity Awards
Deadline: continuous
http://www.jsmf.org/programs/cs/

NSF

Cyber-Enabled Sustainability Science and Engineering (CyberSEES)
Deadline: February 5, 2013
http://www.nsf.gov/funding/pgm_summ.jsp?pims_id=504829

Exploiting Parallelism and Scalability (XPS)
Deadline: February 20, 2013
http://nsf.gov/funding/pgm_summ.jsp?pims_id=504842

Core Techniques and Technologies for Advancing Big Data Science & Engineering (BIGDATA)
Deadline: June 13, 2013
http://www.nsf.gov/funding/pgm_summ.jsp?pims_id=504767

Expeditions in Computing
Deadline: September 10, 2013
http://www.nsf.gov/funding/pgm_summ.jsp?pims_id=503169

Secure and Trustworthy Cyberspace (SaTC)
Deadline: Sep 30, 2013 (medium) / Dec 16, 2013 (small)
www.nsf.gov/funding/pgm_summ.jsp?pims_id=504709

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Call for Papers: Embedded Systems Week (ESWEEK) 2013

Montreal, Canada, September 29 - October 04, 2013
http://esweek.acm.org

++ CASES +++ CODES+ISSS +++ EMSOFT +++ Workshops +++ Tutorials ++

About ESWeek

ESWeek is the premier event covering all aspects of embedded

systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, and EMSOFT), two symposia (ESTIMedia and RSP) and several workshops and tutorials, ESWeek allows attendees to benefit from a wide range of topics covering the state of the art in embedded systems research & development.

Dates

- Abstract submission: March 29, 2013
- Full paper submission: April 05, 2013
- Acceptance notification: July 05, 2013
- Camera ready version: July 26, 2013
- Early Reg. deadline: August 28, 2013
- Conference: Sept 29 - Oct 04, 2013

For instructions on paper submissions as well as call for special sessions and tutorials see: http://esweek.acm.org

Organization

ESWeek General Chairs:
Luca Carloni, Columbia University, USA
Karam S. Chatha, Arizona State University, USA

ESWeek Local Arrangement Chairs:
Gabriela Nicolescu, Polytechnique Montreal, Canada

CASES TPC Chairs:
Rodric Rabbah, IBM, USA
Anand Raghunathan, Purdue University, USA

CODES+ISSS TPC Chairs:
Radu Marculescu, Carnegie Mellon University, USA
Preeti Panda, IIT Delhi, India

EMSOFT TPC Chairs:
Rolf Ernst, TU Braunschweig, Germany
Oleg Sokolsky, University of Pennsylvania, USA

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Call for Submissions: PhD Forum at DAC 2013

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by SIGDA for Ph.D. students to to present an discuss their dissertation research with people in the EDA community. It has become one of the premier forums for Ph.D. students in design automation to get feedback on their research and for industry to see academic work in progress: 400 - 500 people attended the last forums. Participation in the forum is competitive with

acceptance rate of around 30%. Limited funds will be available for travel assistance, based on financial needs. The forum is open to all members of the design automation community and is free-of-charge. It is co-located with DAC to attract the large DAC audience, but DAC registration is not required in order to attend this event.

Eligibility

Students with at least one published or accepted conference, symposium or journal paper. Students within 1-2 years of dissertation completion and students who have completed their dissertation during the 2011-2012 academic year. Dissertation topic must be relevant to the DAC community. Previous forum presenters are not eligible. Students who have presented previously at the DATE and ASP-DAC Ph.D. forums are eligible, but will be less likely to receive travel assistance.

Important Dates

Submission Deadline: March 10, 2013
Submission Link: http://www.easychair.org/conferences/?conf=daforum13
Notification Date: April 15, 2013
Forum Presentation: TBA

Submission Requirements

A two-page PDF abstract of the dissertation (in two-column format, using 10-11 pt. fonts and single-spaced lines), including name, institution, advisor, contact information, estimated (or actual) graduation date, whether the work has been presented at ASP-DAC Ph.D. Forum or DATE Ph.D. Forum, as well as figures, and bibliography (if applicable). The two-page limit on the abstract will be strictly enforced: any material beyond the second page will be truncated before sending to the reviewers. Please include a description of the supporting paper, including the publication forum. A list of all papers authored or co-authored by the student, related to the dissertation topic and included in the two-page abstract, will strengthen the submission.

A published (or accepted) paper, in support of the submitted dissertation abstract. The paper must be related to the dissertation topic and the publication forum must have a valid ISBN number. It will be helpful, but is not required, to include your name and the publication forum on the first page of the paper. Papers on topics unrelated to the dissertation abstract or not yet accepted will not be considered during the review process.

Please Note:

The abstract is the key part of your submission. Write the abstract for someone familiar with your technical area, but entirely unfamiliar with your work. Clearly indicate the motivation of your Ph.D. dissertation topic, the uniqueness of your approach, as well as the potential impact your approach may have on the topic.
In the beginning of the abstract, please indicate to which track your

submission belongs to. Proper spelling, grammar, and coherent organization are critical: remember that the two pages may be the only information about yourself and your PhD research available to the reviewers.
All submissions must be made electronically. Please include the supporting paper with the abstract in one PDF file and submit the single file. There are many free utilities available online which can merge multiple PDF files into a single file if necessary.

Tracks
---
* System-level Design, Synthesis and Optimization (including network-on-chip, system-on-chip and multi/many-core, HW/SW co-design, embedded software issues, modeling and simulation
* High Level Synthesis, Logic Level Synthesis
* Physical Design and Manufacturability
* Power and Reliability Analysis and Optimization (including power management from system level to circuit level, thermal management, process variability management)
* Timing Analysis, Circuit and Interconnect Simulation
* Signal Integrity and Design Reliability, Analog/Mixed Signals and RF
* Verification, Testing, Pre- and Post-Silicon Validation, Failure Analysis
* Reconfigurable and Adaptive Systems
* Emerging Design and Technologies (carbon nanotubes, molecular electronics, MEMS, microfluidic system, biologically-inspired systems, quantum computing, etc.)

Submissions dealing with power modeling, analysis, and/or optimization may be submitted to any track, depending on the abstraction level and contents of the work. Same principle also applies to variability-aware and fault-tolerant design and analysis. Please consult your advisor to determine which track is the best fit for your submission.
If you still have questions about the most appropriate submission track, you are encouraged to contact the TPC Chair, Dr. Shiyan Hu (shiyan@mtu.edu).

Contact Information

For questions not addressed on this page, please send e-mail to Dr. Shiyan Hu: shiyan@mtu.edu. Please include "DAC Ph.D Forum" in the subject line of your email.

Organizing Committee

Shiyan Hu Michigan Technological University
Laleh Behjat University of Calgary
Mircea Stan, University of Virginia
Gi-Joon Nam, IBM Research

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Call for Participation: TAU 2013 Variation Aware Timing Analysis Contest

TAU 2013 (www.tauworkshop.com) invites you to participate in a software tool development contest on variation aware parametric timing analysis. With the increasing number and significance of manufacturing and environmental sources of variability in the design and use of modern VLSI designs, timing analysis considering the uncertainty due to variability is essential. At the same time, the growing complexity of modern designs requires fast timing analysis, thereby requiring tools to adopt accuracy and run-time tradeoffs. The goals of this contest are the following.

* Motivate university level students to learn about modern VLSI design timing analysis in the presence of variability and encourage research in this area
* Provide insight to some challenging aspects of a "fast" parametric (e.g. statistical) static timing analysis tool, and look for novel solutions, the results of which may be interesting to both industry and academia
* Encourage use of parallel techniques for timing analysis (especially multi-threaded techniques)
* Facilitate creation of a public university level variation aware timer (would serve as a framework for contests in future)

Contestants would be asked to additionally provide a presentation (.ppt or .pdf) describing key novel contributions of their tool. The top three contestants would be invited to present their work as part of the TAU-20 talks. Look out for contest details and details on "surprise" awards for the top contestants on the website:

https://sites.google.com/site/taucontest2013/

IMPORTANT DATES

Contest specifications, sample benchmarks, and a cell library are available on the contest website. Upon request, a deterministic timer infrastructure is available.

â€¢ Contest announced: October 12, 2012
â€¢ Early binaries due (for verification/initial feedback): February 1, 2013
â€¢ Final version of binaries due with 2 page document describing key ideas: February 15, 2013
â€¢ Results announced: March 27, 2013 (at TAU workshop)

CONTACT

All communication regarding the TAU 2013 contest (including contest registration) must be directed to tau.contest@gmail.com. Contest organizers:
â€¢ Dr. Debjit Sinha, IBM Corp. (Chair)
â€¢ Prof. Luis Guerra e Silva, INESC-ID / IST - TU Lisbon, Portugal
â€¢ Prof. Jia Wang, Illinois Institute of Technology,
â€¢ Dr. Shesha Ragunathan and Mr. Dileep Netrabile, IBM Corp.
â€¢ Dr. Ahmed Shebaita, Synopsys Inc.

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Notice to Authors

This newsletter is a free service for current SIGDA members and is added automatically with a new SIGDA membership.
Circulation: 2,700